

The logo for GadgEon, with 'Gadg' in blue and 'Eon' in orange.

Engineering Smartness

# CAVIUM THUNDER X BASED SERVER BOARD





## Cavium thunder x based server board



Design, testing and productization of a dual CPU based backplane server board based on CN88XX processor

### Results / Outcomes

- Successfully designed the Cavium Thunder X based server reference platform in single spin.
- Detailed EVT of the product including interface validation of 40G QSFP and 10G SFP+, PCIe3.0 and XAUI interfaces.
- Successfully completed all the certifications of the board.
- Successfully implemented all manufacturing testing including chassis test of the server board.



# System Design and Implementation Details

SI No	Category	Description
2	Interfaces availed	DDR4 RDIMM, 1x QSFP+(40G), 2x SFP+(10G), 1x USB 3.0, 1 x USB1.1, <ul style="list-style-type: none"> <li>1x 10/100/1000 LAN, 1x DB9, 1x VGA,</li> <li>1x X8 PCIe connector on board,</li> <li>1x X24 connector with X8 electrical connection.</li> <li>2X 0.5mm pitch 50 pin back plane connector</li> </ul>
3	Design Challenges	<ul style="list-style-type: none"> <li>Productization of dual chipset server board with a board management controller with ARM 64 powered CPU and 288-pin RDIMM connector</li> <li>Power design involving high current rated programmable buck regulators which source current up to 128A.</li> </ul>
4	Hardware design(Schematics)	<ul style="list-style-type: none"> <li>Complex power section design in adhering to PCIe electro-mechanical spec.</li> <li>Part selection to minimal foot print as possible to accumulate all interfaces in required PCB dimensions.</li> <li>Active heat sink and TIM material selection.</li> </ul>
5	PCB design(Layout)	<ul style="list-style-type: none"> <li>Half height/Half length PCIe card (167x 65mm), 12 layer 1.6mm thick PCB.</li> <li>Routing complexity involving differential pair and group length matching and intra spacing for the PCIe 2.1 Interfaces between Octeon/Nitrox/ Intel chipsets placed on single side of PCB</li> <li>Very high current sourcing power plane cutting for various voltages on board.</li> <li>Highly challenge to achieve all above specification in required form-factor.</li> </ul>
6	Fab and Assembly House co-ordination	<ul style="list-style-type: none"> <li>DFM and DFA reviews</li> <li>Low cost CBOM's with low cost alternates identified for high cost parts, life time check for critical components in design including NAND and NOR flashes</li> <li>Manufacturing support with alternates identified for components going to EOL/obsolesce</li> </ul>
7	Board bring-up and Testing	<ul style="list-style-type: none"> <li>Initial bring-up of the board followed by detailed Electrical interface validation(EVT) including interface validation of XAUI, PCIe interfaces</li> <li>ispPAC(voltage/reset sequencer) programming for power/reset sequencing</li> </ul>



8	Firmware Application development	<ul style="list-style-type: none"><li>• Development of bootloaders for Oction chipset including memory configuration of NOR flash and NAND flash, boot configuration strapping, PCIe configuration etc</li><li>• Development of manufacturing test scripts for board testing.</li><li>• Development of PCIe/XAUI drivers for chipsets</li></ul>
9	Mechanical and 3-D design	<ul style="list-style-type: none"><li>• Prepared the 3-D model of the board.</li><li>• Worked with 3rd party mechanical team for developing heat sink and I/O bezel</li></ul>

# THANK YOU



For More Details, Let's Connect



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